

WHAT IS CLAIMED IS:

1. A method of programming a group of memory cells in parallel, each memory cell having a charge storage individually programmable to a target charge level corresponding to a target memory state among a plurality of memory states  
5 thereof, comprising:

providing a plurality of voltage levels for programming a memory cell to one of said plurality of memory states;

selecting one of said plurality of voltage levels for each memory cell of the group, the selected voltage level being a function of the memory cell's target memory  
10 state;

generating a programming voltage as function of the selected voltage for each memory cell; and

programming the group of memory cells in parallel.

15 2. A method as in 1, further comprising:

generating a programming voltage waveform for each cell of said group, each said programming voltage waveform having an initial amplitude which is a function of said voltage level selected for each cell.

20 3. A method as in 2, wherein said programming voltage waveform includes a series of voltage pulses.

4. A method as in 3, wherein applying an initial one of said series of voltage pulses programs each cell substantially towards but not overshooting its target  
25 memory state.

5. A method as in 3, wherein said series of voltage pulses has an amplitude that increases with time.

30 6. A method as in 3, further comprising:

(a) programming said group of memory cells in parallel by applying to each cell a pulse from said series of voltage pulses of the programming voltage waveform associated with each cell;

(b) verifying said group of memory cells in parallel by determining if each cell has been programmed to a predetermined level associated with the target state of each memory cell,

5 (c) inhibiting any cell from said group from further programming when said any cell has been programmed to its predetermined level; and

(d) repeating (a), (b) and (c) until all cells in said group have been programmed to their respective predetermined levels.

10 7. A method as in 6, wherein said repeating step also terminates when it has iterated more than a predetermined number of times.

15 8. A method as in 6, wherein said repeated cycling of (a)-(d) until termination constitutes one programming phase, and said method further comprises one or more additional programming phases, each with its associated series of voltage pulses and predetermined levels.

9. A method as in 8, wherein each successive phase employs a series of voltage pulses that produce a finer programming step from the previous phase.

20 10. A method as in 8, wherein each successive phase employs predetermined levels that are closer to the target states.

25 11. A method as in 8, wherein a predetermined last phase employs predetermined levels that have each cells of the group programmed to their respective target states.

12. A method as in 8, wherein each cell receives no more than twenty programming pulses.

30 13. A method as in anyone of claims 1-12, wherein each cell stores one of two memory states.

14. A method as in anyone of claims 1-12, wherein each cell stores more than two memory states.

15. A method as in anyone of claims 1-12, wherein each cell stores one of  
5 sixteen memory states.

16. A nonvolatile memory, comprising:  
an array of memory cells, each memory cell having a charge storage individually programmable to an associated target charge level corresponding to a  
10 target memory state among a plurality of memory states thereof;  
a power bus supplying a plurality of voltages in parallel for programming a memory cell to one of said plurality of memory states; and  
a parallel programming system for programming a group of memory cells in parallel, said parallel programming system having a plurality of programming  
15 circuits, one for each cell in the group, each programming circuit further comprising:  
a voltage selector selecting one of the plurality of voltages from said power bus, the selected voltage being a function of the target state of the associated memory cell such that the selected voltage is optimum for said programming circuit to produce a programming voltage for programming the memory state towards its target memory  
20 state.

17. A nonvolatile memory as in 16, wherein said programming circuit further comprising:  
a first programming voltage waveform generator coupled to receive said  
25 selected voltage to generate a first programming voltage waveform having an initial amplitude which is a function of the selected voltage;  
a sense amplifier for determining the programmed state of the memory cell;  
and  
a program inhibit circuit responsive to the sense amplifier for inhibiting  
30 further programming of the cell whenever the programmed state of the memory cell has passed a first predetermined level.

18. A non-volatile memory as in 17, further comprising:

a storage element for saving the last programming voltage that causes the programmed state of the associated cell to pass the first predetermined level;

a second programming voltage waveform generator responsive to said last programming voltage saved for generating a second programming voltage; and

- 5 a controller for enabling said second programming voltage waveform generator after all memory cells in the group have passed the first predetermined level.